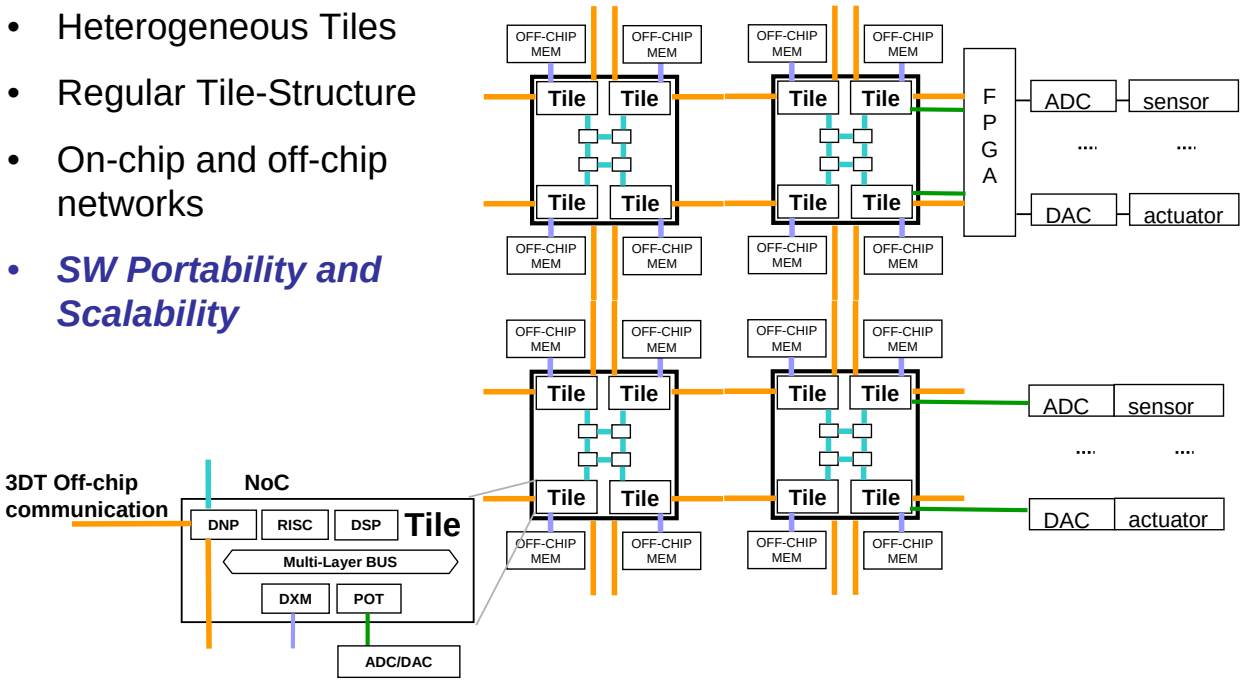
# Closing the Loop
# Exploration and Estimation

***Lothar Thiele***, Iuliana Bacivarov, Wolfgang Haid, Kai Huang

ETH Zurich, Switzerland

# A Sample HW Architecture (EU-SHAPES)

- Heterogeneous Tiles
- Regular Tile-Structure
- On-chip and off-chip networks
- ***SW Portability and Scalability***



## Some Challenges in MPSoC Programming

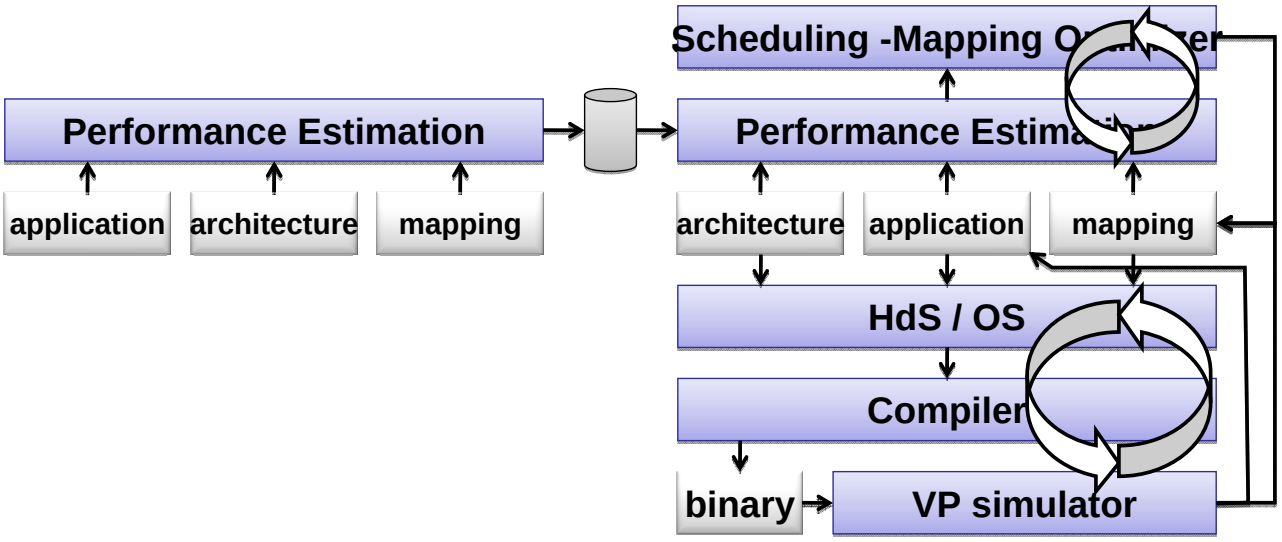
- Design Process
- Programming Model
- Optimization
- Scalability
- Calibration



## Some Challenges in MPSoC Programming

- **Design Process**
- **DOL (Distributed Operation Layer)**
- Programming Model
- Optimization
- Scalability
- Calibration

# DOL Design Flow






# Some Challenges in MPSoC Programming

- Design Process
- **Programming Model**
- Optimization
- Scalability
- Calibration

- DOL (**D**istributed **O**peration **L**ayer)
- **Process networks and explicit communication**

# Application Specification

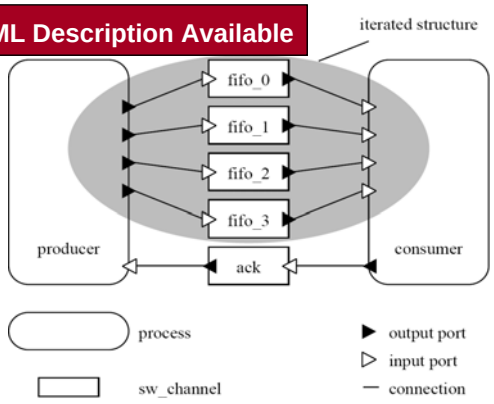
## Structure

- **Process Network**
  - Processes
  - SW channels (FIFO behavior)
- **Iterators**
  - Scalability for processes, SW channels, entire structures

## Functional specification

- **Language:** C/C++
- **API:** DOL primitives

**XML Description Available**




**Algorithm 1** Process Model

```
1: procedure INIT(DOLProcess p)                ▷ initialization
2:     initialize local data structures
3: end procedure

4: procedure FIRE(DOLProcess p)                ▷ execution
5:     DOL_read(INPUT, size, buf)              ▷ blocking read
6:     manipulate
7:     DOL_write(OUTPUT, size, buf)            ▷ blocking write
8: end procedure
```



# Scalability at Specification Level

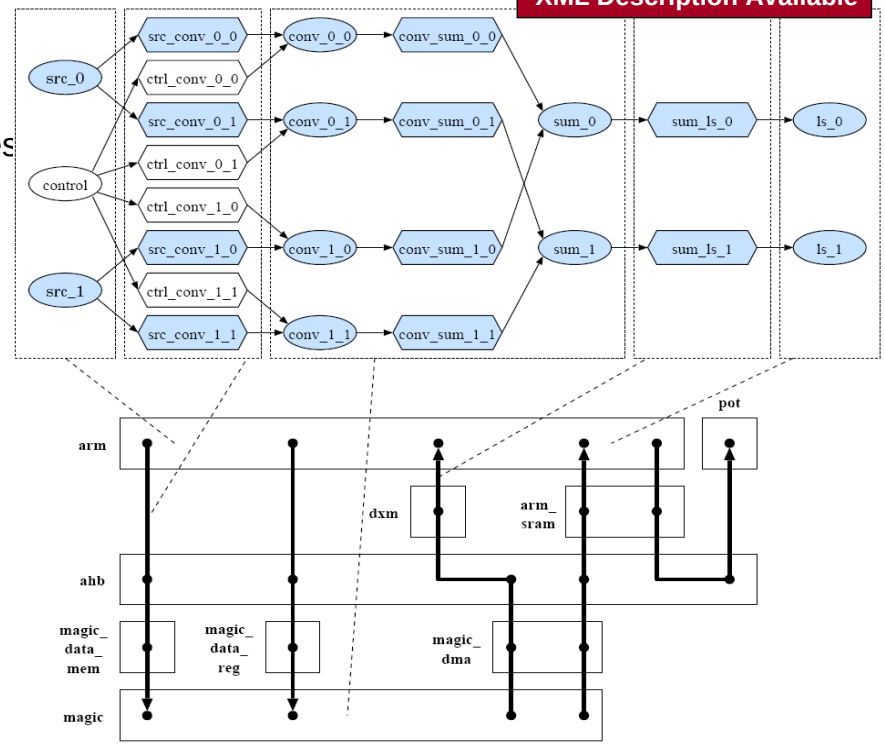
- Separation of instruction/thread level parallelism (inside processes) and process-level parallelism.
- Use of iterators in
  - architecture specification
  - application specification
  - mapping specification

$$\{(i,j) : 1 \leq i \leq N \wedge i \leq j \leq N\}$$

# Mapping Specification

XML Description Available

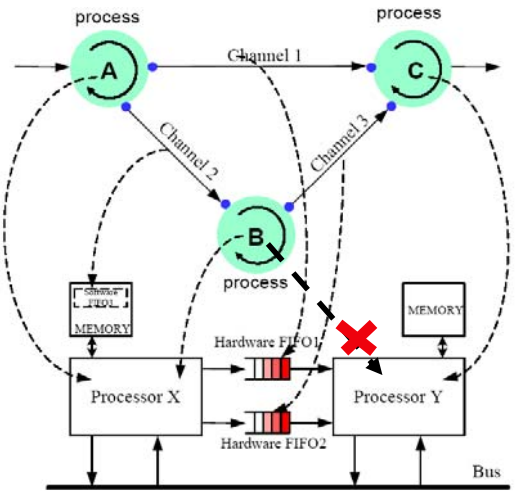
- **Binding**
  - Processes to execution resources
  - SW channels to read/write paths
- **Scheduling**
  - Processors
  - Communication
- **Constraints**
  - To be considered during HdS generation






# Mapping Constraints

- Certain processes must run on certain processors or processor types
- Some processes must be mapped to the same processor
- Some communication must be mapped onto specific paths
- Restrictions on resource sharing policies



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- Process networks and explicit communication
- ***Hybrid* black-box methods**



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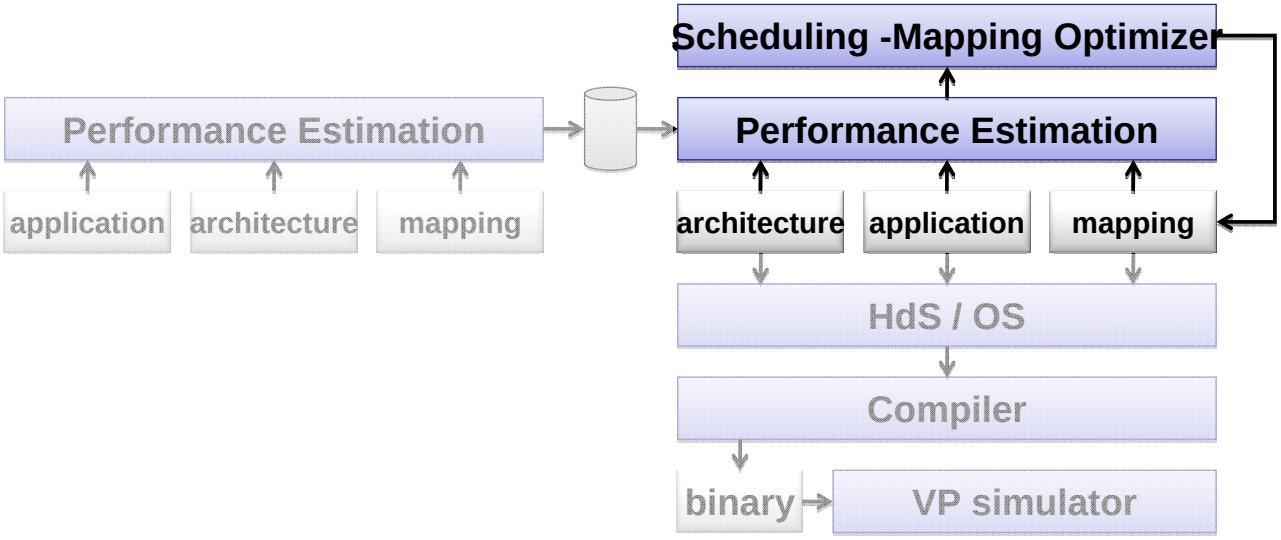

# Design Space Exploration Framework

- **PISA&EXPO**
  - multi-objective optimization using evolutionary algorithms
  - [PISA] https://www.tik.ee.ethz.ch/pisa;
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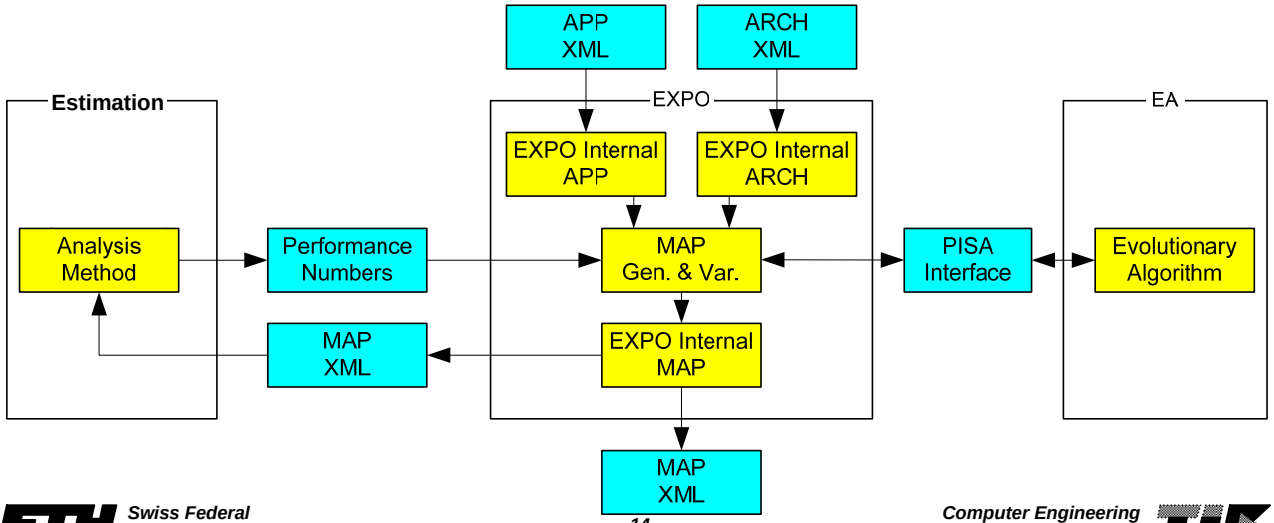




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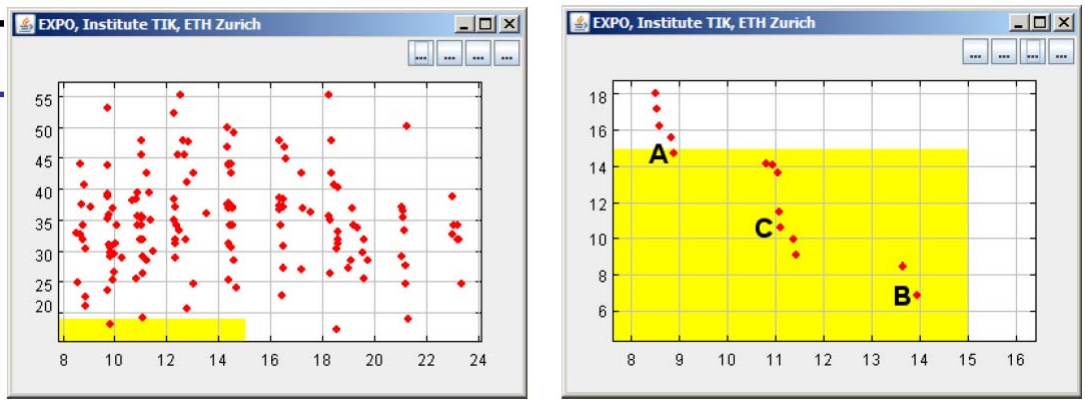
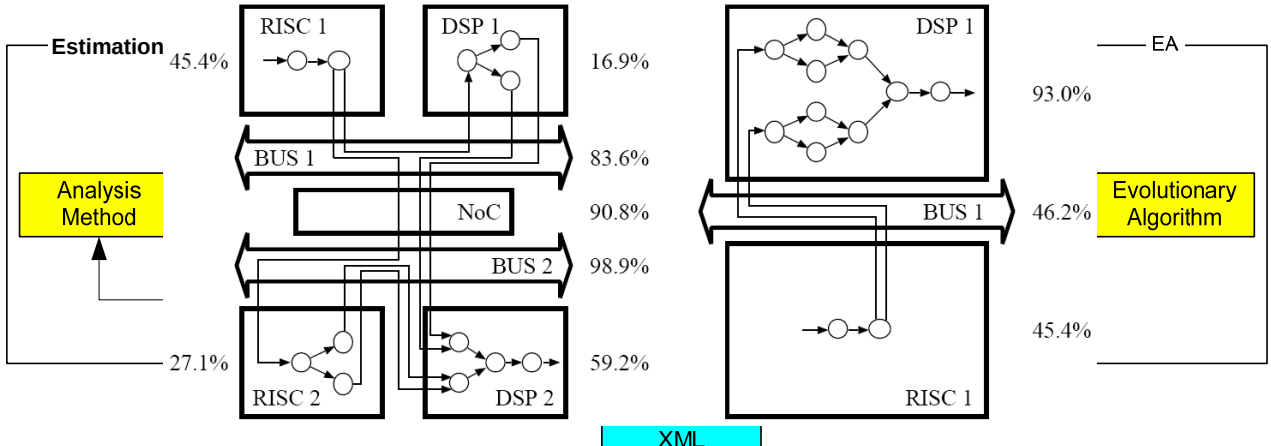
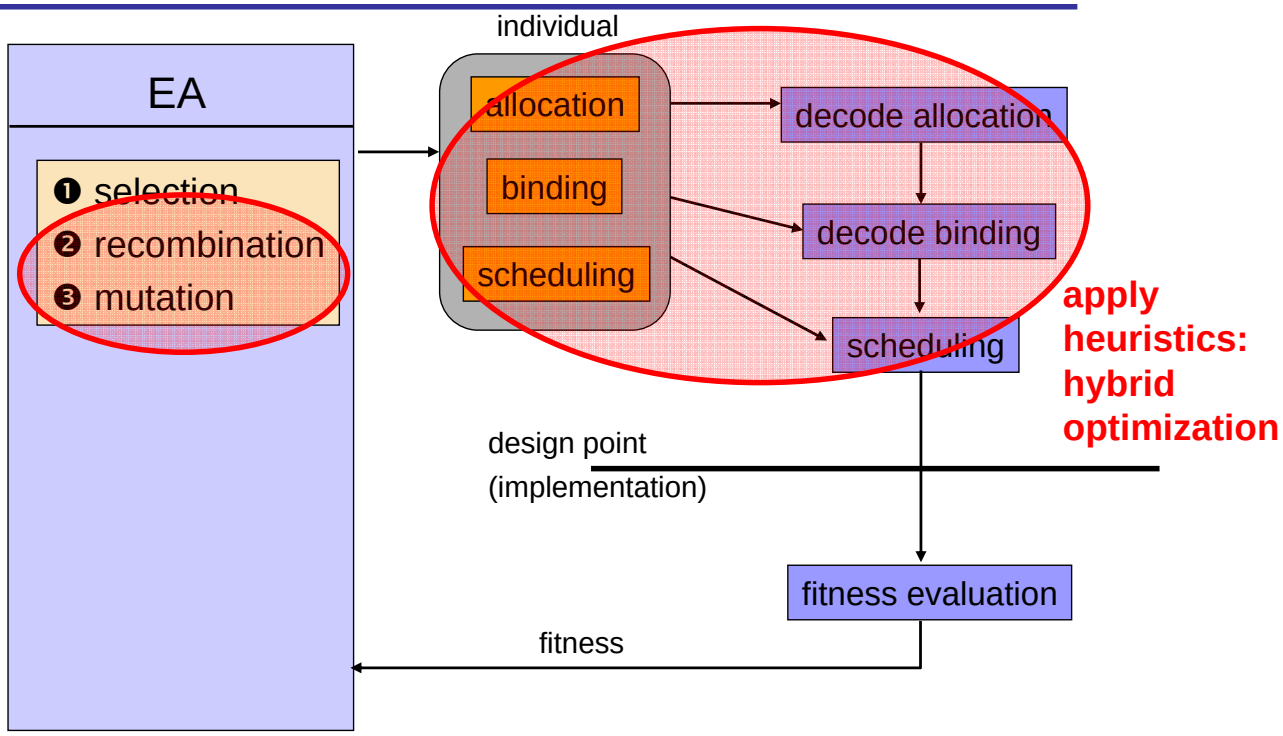


# Evolutionary Algorithms for DSE



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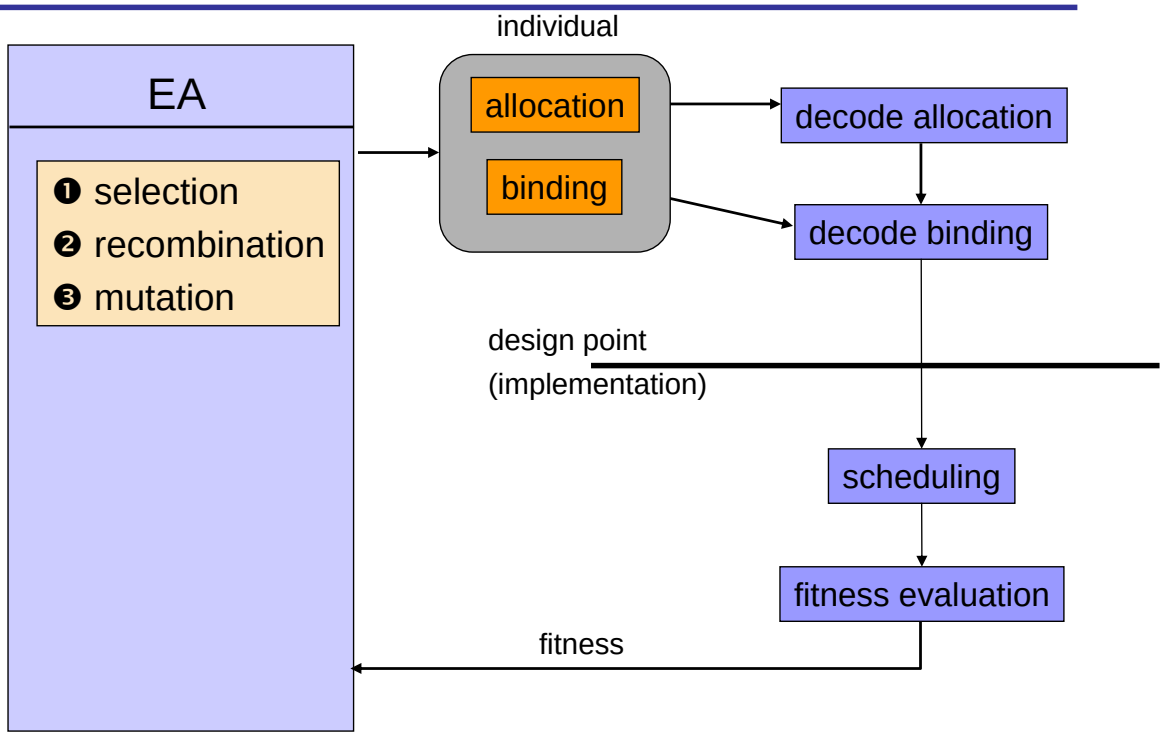

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- **Multi-level performance estimation**



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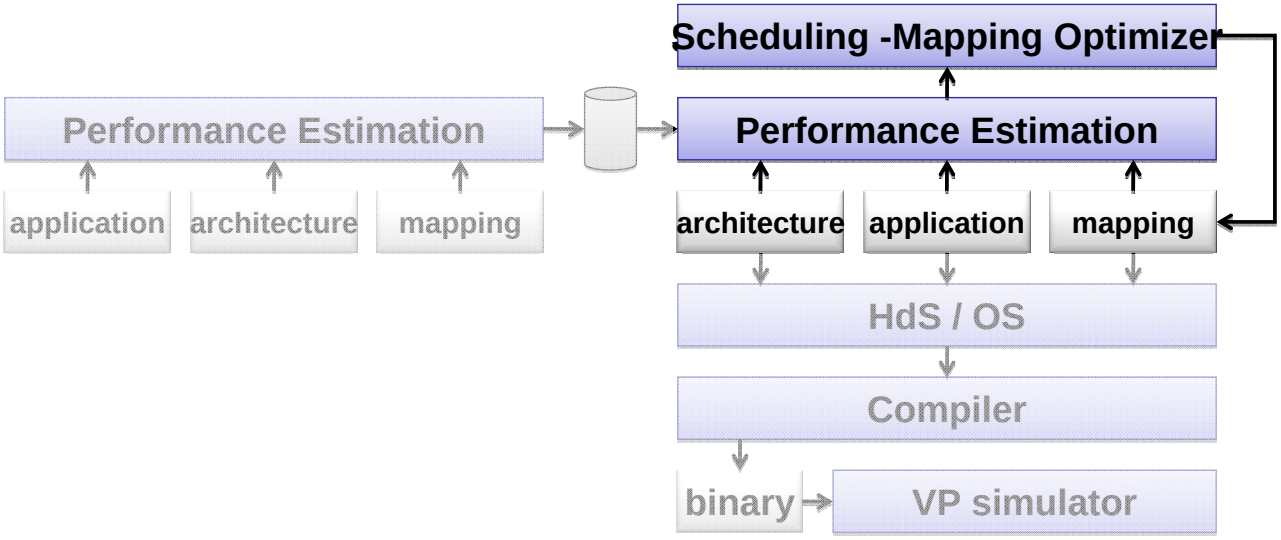


# Additive Model

processor c with worst total runtime

number of firings of task p

runtime of task p on processor c

$$obj_1 = \max_{c \in \mathcal{C}} \left\{ \sum_{\forall p \text{ mapped to } c} n(p) \cdot r(p,c) \right\}$$

communication link with worst load

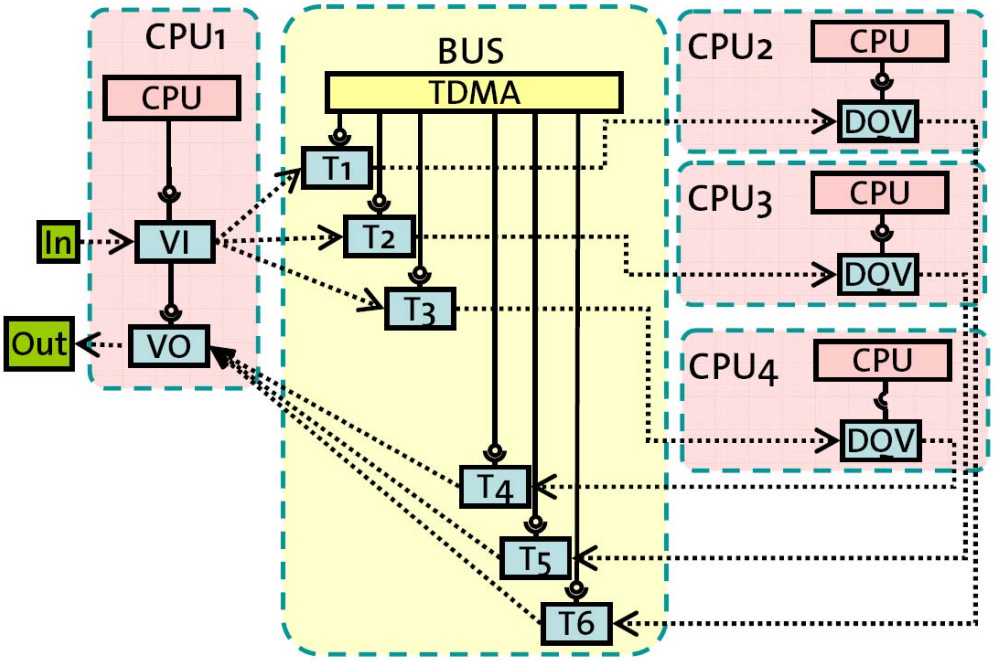
communication request from channel s

bandwidth of communication link g

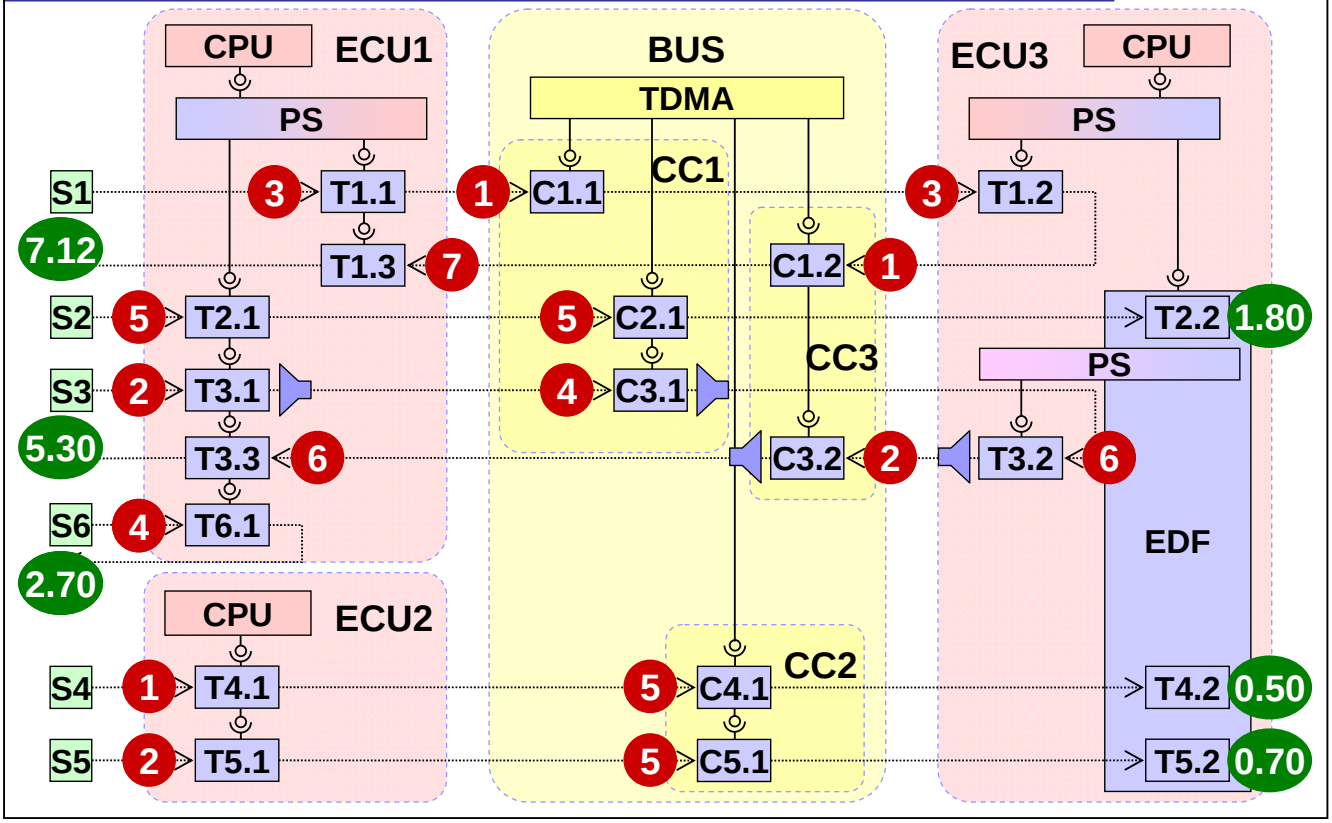
$$obj_2 = \max_{g \in \mathcal{G}} \left\{ \sum_{\forall s \text{ mapped onto } g} \frac{b(s)}{t(g)} \right\}$$



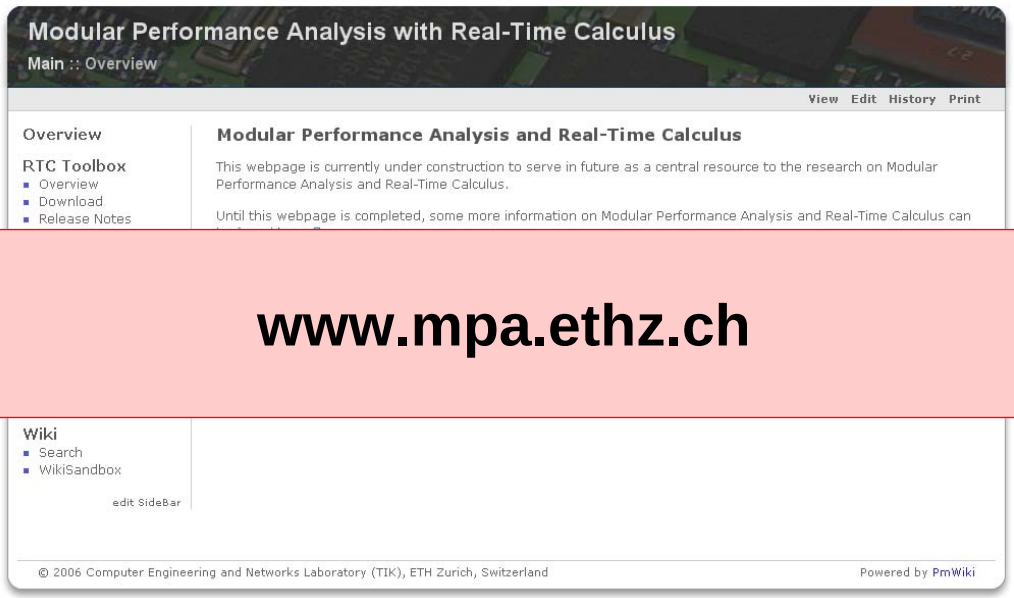
# MPA Performance Model



# A More Complex Scenario



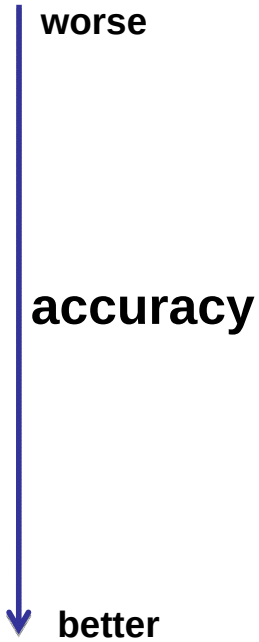

# Performance Analysis - RTC Toolbox




**www.mpa.ethz.ch**

# Run-time Comparison

- **Additive Model**
  - Generation: < 0.1s; Analysis: < 0.1s
- **Modular Performance Analysis**
  - Generation: 0.5s; Analysis: 2s
- **Functional Simulation**
  - Generation: 35s ; Simulation: 3s
- **Virtual Platform Simulation**
  - Generation: 170s; Simulation: 1300s



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- **Reference points**

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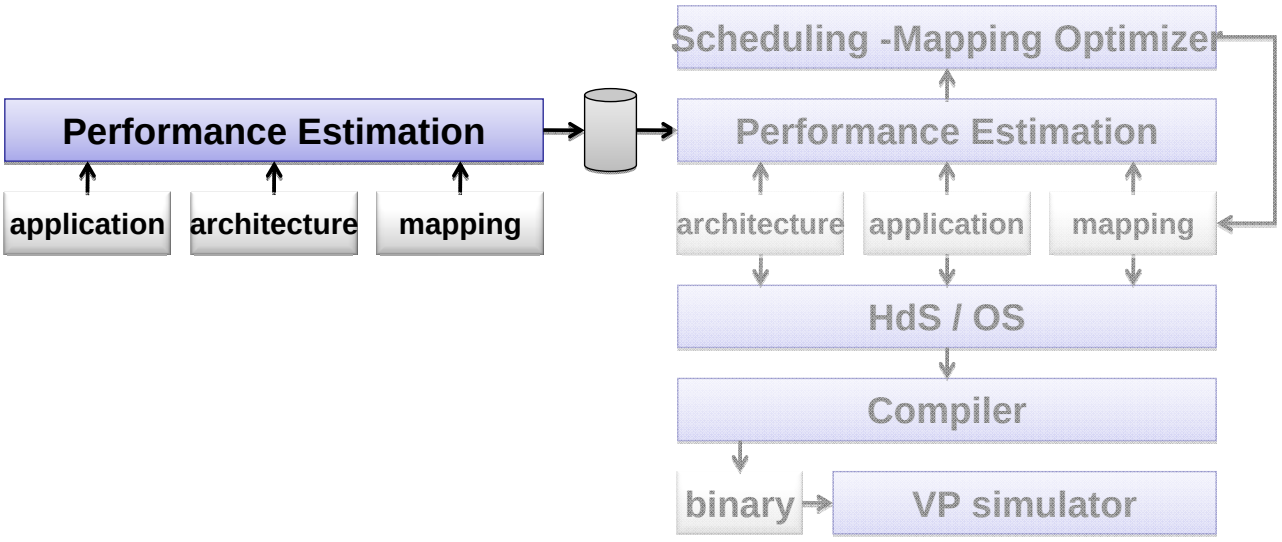




# Reference Points

- **Data sheets**
  - basic platform characteristics, bounds on delay, throughput, …
- **Functional Simulation**
  - communication volume, number of task invocations, …
- **Platform Benchmarks**
  - map benchmark applications to platform for profiling the OS, communication services, network, … .
- **Sample Mappings**
  - map the application to the platform in a limited number of settings
  - estimations on execution times

# DOL Design Flow